24. A method for fabricating a semiconductor device according to claim 10, wherein the fourth ion implanted layer is formed into the surface part of the semiconductor region by implanting indium ions. --

REMARKS

The Examiner's Final Office Action dated November 18, 2002 has been received and its contents reviewed. Applicants would like to thank the Examiner for the consideration given to the above-identified application.

Claims 6-15 were pending in the present application for consideration, and claims 1-5 have been withdrawn from consideration in response to the Election/Restriction Requirement filed January 14, 2002. By this Amendment, claim 6 has been amended, and claims 20-24 have been added. Accordingly, claims 6-15 and 20-24 are pending for consideration, of which claim 6 is independent.

Referring now to the detailed Office Action, the Examiner objects to the Amendment filed September 5, 2002 under 35 U.S.C. §132 as introducing new matter. The Examiner asserts the original disclosure does not support the features wherein "the heavy ions are implanted at such an implant energy as getting a range of the heavy ions located inside the extended high-concentration dopant diffusion layer". Further, claim 11 stands rejected under 35 U.S.C. §112, first paragraph, as containing subject matter not described in the specification. Particularly, this rejection follows the reasoning of the §132 objection summarized above. These objection and rejection are respectfully traversed for the reason that support for the claimed feature can be found in the description in page 16, lines 18-20 of the present specification, which discloses that the pocket dopant diffused layer in contact with the lower portion of the extended high-concentration dopant diffused layer is formed after the heat treatment. In view of the arguments set forth above, the §132 objection and the §112, first paragraph, rejection are respectfully requested to be reconsidered and withdrawn.

As claim 11 has been canceled, the rejection is rendered as moot. Applicants respectfully submit that new claim 22, which correspond to canceled claim 11, is supported in page 22, lines 21-23 of the present application.

Claims 6-13 stand rejected under 35 U.S.C. §102(b) as anticipated by Burr (U.S. Patent No. 5,923,987). Further, claim 14 stands rejected under 35 U.S.C. §103(a) as unpatentable over Burr, and claim 15 stands rejected under 35 U.S.C. §103(a) as unpatentable over Burr in view of Tsukamoto (U.S. Patent No. 5,399,506). These rejections are respectfully traversed at least for the reasons provided below and the claim amendments set forth above.

The amended claim 6 of the present invention recites a method for fabricating a semiconductor device that includes an extended high-concentration dopant diffused layer of a first conductivity and a pocket dopant diffused layer of a second conductivity, including: a second step of implanting heavy ions into the semiconductor region on both sides of the gate electrode using the gate electrode as a mask, thereby forming a first ion implanted layer of the second conductivity, at least upper part of which is an amorphous layer; a third step of implanting ions of a first dopant into the semiconductor region, in which the amorphous layer has been formed, using the gate electrode as a mask, thereby forming a second ion implanted layer of the first conductivity type; and a fourth step of conducting a first annealing process to activate the first and second ion implanted layers, thereby forming the extended high-concentration dopant diffused layer of the first conductivity type through diffusion of the first dopant the pocket dopant diffused layer of the second conductivity type, which is in contact with a bottom portion of the extended high-concentration dopant diffused layer, through diffusion of the heavy ions, respectively, wherein the pocket dopant diffused layer includes, in a portion in contact with the extended high-concentration dopant diffused layer, a segregated part that has been formed through segregation of the heavy ions.

Accordingly, since heavy ions are used to form the pocket dopant diffused layer of the second conductivity type, pre-amorphization effects are attainable by the implantation of the heavy ions. Further, the dislocation loop layer can advantageously trap the silicon interstitials.

In addition, since heavy ions are easily trapped and segregated in the dislocation loop layer, the extended high-concentration dopant diffused layer and pocket dopant diffused layer can both have their junctions shallowed and sharpened. Accordingly, a miniaturized semiconductor device can be provided with the inverse channel effects suppressed.

Burr teaches a method for forming a MOS device including the steps of:

1) forming a gate oxide film 340 and a gate electrode layer 342 on a silicon substrate 332, as shown in, e.g., Fig. 5F;

2) forming a mask 326 covering the substrate from the gate electrode 342 along a drain region (right side), and thereafter, using the gate electrode layer 342 and the mask 326 as a mask, forming a pocket region 347 by ion implanting p-type dopant , as disclosed in, e.g., Fig. 5);

3) forming n doped layers 336A and 336B by ion implanting n-type dopant using the gate electrode 342 as a mask (see Fig. 5H).

Hence, Burr discloses using indium as a pocket dopant.

According to the amended claim 6 of the present invention, during the forming of the pocket dopant diffused layer of the second conductivity type, heavy ions are implanted into the semiconductor region on both sides of the gate electrode using the gate electrode as a mask. Hence, the extended high-concentration dopant diffused layer and pocket dopant diffused layer can both have their junctions shallowed and sharpened.

However, according to Fig. 5G of Burr, the pocket region 347 is merely formed in the source region side (left side) using the gate electrode 342 and the mask 326 as a mask. Hence, Burr fails to disclose forming the pocket dopant diffused layer in the semiconductor region on both sides of the gate electrode, such as in the presently claimed invention.

The Examiner asserts that, as shown in Fig. 5H, Burr discloses that the pocket region 347 includes a segregated part that has been formed through segregation of the heavy ions. However, Fig. 5H of Burr merely shows the pocket region 347 directly after ion implantation and fails to show that a segregated part is included therein. The segregated part is formed due to heat treatment and not formed directly after ion implantation. Moreover, in Fig. 5H, since the pocket dopant is boron, even if a heat treatment is performed, Applicants respectfully assert that no segregated part will be formed.

In addition, even if indium is used as the pocket dopant, a segregated part can only be formed due to heat treatment when the dosage is $5 \times 10^{13}cm^{-2}$ or more. However, according to Burr, since the dosage of the pocket region 347 is between 5×10^{11} and $1 \times 10^{13}cm^{-2}$, the segregated part cannot be formed.

The Examiner also asserts that the technique of forming an amorphous semiconductor substrate by implanting heavy ions is well known. However, even if indium is used as the pocket dopant, an amorphous layer can only be formed when the dosage is 5 X $10^{13}cm^{-2}$ or more. Further, since the dosage of the pocket region 347 is between 5 X 10^{11} and 1 X $10^{13}cm^{-2}$, the amorphous layer cannot be formed.

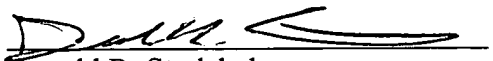
For the foregoing reason, Applicants claimed invention are distinguishable over Burr, and the rejections under §102 and §103 are respectfully requested to be reconsidered and withdrawn.

New dependent claims 20-24 have been added to further complete the scope of the invention to which Applicants are entitled.

CONCLUSION

Having responded to the rejection set forth in the outstanding Final Office Action, it is submitted that claims 6-10, and 12-15 and new claims 20-24 are now in condition for allowance. An early and favorable Notice of Allowance is respectfully solicited. In the event that the Examiner is of the opinion that a brief telephone or personal interview will facilitate allowance of one or more of the above claims, the Examiner is courteously requested to contact Applicants' undersigned representative.

Respectfully submitted,



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MARKED-UP VERSION OF AMENDED CLAIMS:

6. (Twice Amended) A method for fabricating a semiconductor device that includes an extended high-concentration dopant diffused layer of a first conductivity and a pocket dopant diffused layer of a second conductivity, comprising:

a first step of forming a gate electrode over a semiconductor region with a gate insulating film interposed therebetween;

a second step of implanting heavy ions into the semiconductor region on both sides of the gate electrode using the gate electrode as a mask, thereby forming a first ion implanted layer of the second conductivity, at least upper part of which is an amorphous layer;

a third step of implanting ions of a first dopant into the semiconductor region, in which the amorphous layer has been formed, using the gate electrode as a mask, thereby forming a second ion implanted layer of the first conductivity type; and

a fourth step of conducting a first annealing process to activate the first and second ion implanted layers, thereby forming the extended high-concentration dopant diffused layer of the first conductivity type through diffusion of the first dopant and the pocket dopant diffused layer of the second conductivity type, which is [located under] in contact with a bottom portion of the extended high-concentration dopant diffused layer, through diffusion of the heavy ions, respectively,

wherein the pocket dopant diffused layer includes, in a portion in contact with the extended high-concentration dopant diffused layer, a segregated part that has been formed through segregation of the heavy ions.